IN THE DRAWINGS

Please amend Figs. 4 and 5 as illustrated in the provided sheets each labeled "Replacement Sheet." Please note that Fig. 4 has been amended by replacing the reference numeral associated with the wordline with the reference numeral "419", and Fig. 5 has been amended to fix the misspelling of the word "spacer", as highlighted in the Office Action.

REMARKS

Claims 1-31 are pending. Claims 1, 4 and 13 are amended with this response. Applicants note with appreciation the allowance of claims 21-31 and the provisional allowance of claims 12 and 13. Reconsideration of the application is respectfully requested in light of the comments below.

I. OBJECTIONS TO THE SPECIFICATION

Various objections were raised with respect to the specification. Amendments have been made to the drawings, the specification, and the claims in accordance with the highlighted objections. Accordingly, withdrawal of the objections is respectfully requested.

II. REJECTION OF CLAIMS 1-8, 14-16 AND 20 UNDER 35 U.S.C. § 103(a)

Claims 1-8, 14-16 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,524,913 (Lin et al.) in view of U.S. Patent No. 5,418,176 (Yang et al.). Withdrawal of this rejection is respectfully requested for at least the following reasons.

i. Neither Lin et al. nor Yang et al. teach or suggest removing the entire patterned hardmask and the associated spacers, as recited in claim 1.

Claim 1 is directed to a method of forming a portion of a dual bit memory core array. The method comprises forming a patterned hardmask and spacers adjacent the patterned hardmask to define a second spacing between neighboring spacers. A bitline implant is then performed into the underlying substrate through the second spacing to form a buried bitline. The ***hardmask and spacers are then removed entirely*** and a wordline material is then formed and patterned to form a wordline that overlies the buried bitline. Neither Lin et al. nor Yang et al. teach or suggest this claim feature.

Lin et al. teach forming a memory device with a patterned conductive gate

material 240. Spacers 241 are formed adjacent the conductive gate and a bitline implant is performed to form a buried bitline 250, as illustrated in Fig. 2C. Subsequently, as illustrated in Fig. 2D, ***the conductive gate material is selectively patterned to form electrically isolated conductive gate regions 240a*** in a buried bitline direction. The electrically isolated gate regions 240a are then covered with a dielectric material 252 that is planarized, and another conductive layer is deposited and patterned to form conductive wordlines 254, as illustrated in Fig. 2E. The conductive wordlines 254 run perpendicular to the bitlines 250 and individually make contact to the isolated gate regions 240a thereunder, such that gate regions 240a along a given bitline 250 are associated with different wordlines 254. ***As can be seen from Lin et al., to the extent that the conductive gate regions 240 and used as a hardmask for the buried bitline implant, the conductive regions 240 are patterned selectively, and are not removed entirely as claimed.*** Yang et al. do not remedy the deficiency in Lin et al., and therefore claim 1 is nonobvious over the cited art.

ii. One of ordinary skill in the art would not have been motivated to modify Lin et al. in accordance with the present invention because doing so would render the memory device of Lin et al. inoperable.

It is well established that no motivation exists for a modification of a reference if such a modification would render the prior art unsatisfactory for its intended purpose. MPEP § 2143.01 (*citing* In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984)). It is respectfully submitted that a modification of Lin et al. ***to completely remove the patterned hardmask*** prior to forming the conductive wordlines as recited in claim 1 is improper because such a change would render the device inoperable, as will be further explained below.

As highlighted above, Lin et al. form conductive gate regions 240 that extend in the bitline direction, as illustrated in Fig. 2A. After performing a bitline implant, Lin et al. selectively pattern the conductive gates again (forming regions 240a) to isolate individual memory cells along a given bitline, as illustrated in Fig. 2D. Subsequently, a

conductive layer is formed and patterned transverse to the bitline direction to form individual wordlines, that selectively contact the memory cells *via* the conductive gates 240a, such that memory cells along a given bitline are associated with different wordlines, as illustrated in Fig. 2E. If one of ordinary skill in the art would remove the gate regions 240 ***entirely*** at Fig. 2D (instead of ***selectively*** as shown), the subsequently formed wordlines 254 would not be able to contact the memory cells, thereby rendering the memory inoperable. Further, by completely removing the gate regions 240, the memory cells would not even be formed, since no control gate would exist for programming or reading thereof. Therefore no motivation exists for a modification of Lin et al. in accordance with the present invention because such a modification would frustrate the primary purpose of the prior art reference. Thus the present invention is nonobvious over the cited art for at least this additional reason; accordingly, withdrawal of the rejection is respectfully requested.

III. REJECTION OF CLAIMS 9-11 UNDER 35 U.S.C. § 103(a)

Claims 9-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin et al. and Yang et al., and further in view of Cheng-Sheng et al. (1990 IEEE article entitled "A Scaling Methodology for Oxide-Nitiride-Oxide Interpoly Dielectric for EPROM Applications.). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 9-11 rely upon independent claim 1. As highlighted above, neither Lin et al. nor Yang et al. either alone or in combination teach the present invention. Cheng-Sheng et al. fail to remedy the deficiency in the primary references. Therefore claims 9-11 are also nonobvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

IV. REJECTION OF CLAIMS 17-19 UNDER 35 U.S.C. § 103(a)

Claims 17-19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. and Yang et al., and further in view of U.S. Patent 6,884,681 (Kamal et al.).

Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 17-19 rely upon independent claim 1. As highlighted above, neither Lin et al. nor Yang et al. either alone or in combination teach the present invention. Kamal et al. fail to remedy the deficiency in the primary references. Therefore claims 17-19 are also nonobvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

V. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP798US.

Respectfully submitted,
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CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: May 24, 2005 Christine Gillroy

Christine Gillroy

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